AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (currently amended). A computer-implemented method for use in a computer system including a memory, the memory including a plurality of bits tangibly embodied in the memory at a plurality of positions, the method comprising steps of:

(A) identifying the position of a bit in a set of *n* consecutive defective bits tangibly embodied in the memory;

(B) generating an entry in a shift redundancy record indicating that the bit identified in step (A) is defective, the entry and the shift redundancy record being tangibly embodied in a shift redundancy circuit; and

(C) generating a hint record indicating the number *n* of bits in the set of consecutive defective bits, the hint record being tangibly embodied in the shift redundancy circuit.

Claim 2 (original). The method of claim 1, wherein $n=1$.

Claim 3 (original). The method of claim 1, wherein $n=2$.

Claim 4 (currently amended). The method of claim 1, wherein step (A) comprises a step of identifying a defective bit that is tangibly embodied in the memory and adjacent to a functional bit tangibly embodied in the memory; and wherein the method further comprises a step of:

(D) performing steps (A)-(C) for a plurality of sets of consecutive defective bits tangibly embodied in the memory.

Claim 5 (currently amended). The method of claim 1, wherein the step (B) comprises a step of generating a single-bit entry tangibly embodied in the shift redundancy record indicating that the bit identified in step (A) is defective.

Claim 6 (original). The method of claim 1, wherein the memory further comprises a plurality of input/output ports for accessing the plurality of bits, and wherein the method further comprises steps of:

(D) controlling switching circuitry to disconnect the set of *n* consecutive defective bits from the input/output ports.

Claim 7 (currently amended). The method of claim 1, wherein step (C) comprises a step of generating a hint record tangibly embodied in the shift redundancy circuit and representing the value *n*-1.

Claim 8 (currently amended). A computer-implemented method for use in a computer system including a memory, the memory including a plurality of bits tangibly embodied in the memory at a plurality of positions and a plurality of input/output ports for accessing the plurality of bits, the method comprising steps of:

(A) identifying the position of a bit in a set of *n* consecutive defective bits tangibly embodied in the memory, wherein the identified is adjacent to a functional bit tangibly embodied in the memory;

(B) generating a single-bit entry in a shift redundancy record indicating that the bit identified in step (A) is defective, the entry and the shift redundancy record being tangibly embodied in a shift redundancy circuit;

(C) generating a hint record tangibly embodied in the shift redundancy circuit and representing the value *n*-1;

(D) performing steps (A)-(C) for a plurality of sets of consecutive bits tangibly embodied in the memory; and

(E) controlling switching circuitry to disconnect the set of *n* consecutive defective bits from the input/output ports.

Claim 9 (currently amended). An apparatus for use in a computer system including a memory, the memory including a plurality of bits tangibly embodied in the memory at a plurality of positions, the apparatus comprising:

means for identifying the position of a bit in a set of *n* consecutive defective bits tangibly embodied in the memory;

means for generating an entry in a shift redundancy record indicating that the bit identified in step (A) is defective, the entry and the shift redundancy record being tangibly embodied in a shift redundancy circuit; and

means for generating a hint record indicating the number *n* of bits in the set of consecutive defective bits, the hint record being tangibly embodied in the shift redundancy circuit.

Claim 10 (currently amended). The apparatus of claim 9, wherein the means for generating comprises means for generating a single-bit entry tangibly embodied in the shift redundancy record indicating that the bit identified by the means for identifying is defective.

Claim 11 (original). The apparatus of claim 9, wherein the memory further comprises a plurality of input/output ports for accessing the plurality of bits, and wherein the apparatus further comprises:

means for controlling switching circuitry to disconnect the set of *n* consecutive defective bits from input/output ports.

Claim 12 (currently amended). The apparatus of claim 9, wherein the means for generating comprises means for generating a hint record tangibly embodied in the shift redundancy circuit and representing the value *n*-1.

Claim 13 (currently amended). A computer-implemented method for use in a computer system including a first memory and a second memory, the first memory including a plurality of bits tangibly embodied in the first memory at a plurality of positions, wherein b[i] refers to the bit at position i in the plurality of bits, the method comprising steps of:

(A) selecting a first value for a current shift redundancy record variable tangibly embodied in the second memory, wherein the current shift redundancy record value may be toggled between the first value and a second value;

(B) for each of a plurality of consecutive values of i, performing steps of:

(1) if bit b[i] is defective and bit b[i-1] is functional, performing steps of:

(a) toggling the value of the current shift redundancy record variable;

(b) identifying a set of *n* consecutive defective bits tangibly embodied in the first memory and including bit b[i];

(c) tangibly storing in a shift redundancy circuit a hint value in a hints record entry corresponding to bit b[i], the hint value indicating the number *n*; and

(2) tangibly storing the current shift redundancy record value in the shift redundancy circuit in a shift redundancy record element corresponding to bit b[i].

Claim 14 (original). The method of claim 13, wherein *n*=1.

Claim 15 (original). The method of claim 13, wherein n=2.

Claim 16 (currently amended). The method of claim 13, wherein the step (B)(2) comprises a step of tangibly storing a single-bit value in the shift redundancy record representing the position of bit b[i].

Claim 17 (original). The method of claim 13, wherein the step (B)(1) further comprises a step of:

(B)(1)(d) controlling switching circuitry to disconnect the set of n consecutive defective bits from input/output ports of the memory.

Claim 18 (original). The method of claim 13, wherein the hint value is equal to n-1.

Claim 19 (currently amended). A computer-implemented method for use in a computer system including a first memory and a second memory, the first memory including a plurality of bits tangibly embodied in the first memory at a plurality of positions, wherein b[i] refers to the bit at position i in the plurality of bits, the method comprising steps of:

(A) selecting a first value for a current shift redundancy record variable tangibly embodied in the second memory, wherein the current shift redundancy record value may be toggled between the first value and a second value;

(B) for each of a plurality of consecutive values of i, performing steps of:

(1) if bit b[i] is defective and bit b[i-1] is functional, performing steps of:

(a) toggling the value of the current shift redundancy record variable;

(b) identifying a set of *n* consecutive defective bits tangibly embodied in the first memory and including bit b[i];

(c) tangibly storing in a shift redundancy circuit a hint value representing the value *n*-1 in a hints record entry corresponding to bit b[i];

(d) controlling switching circuitry to disconnect the set of *n* consecutive defective bits from input/output ports of the memory; and

(2) tangibly storing the current shift redundancy record value in the shift redundancy circuit in a single-bit

shift redundancy record element corresponding to bit b[i].

Claim 20 (original). An apparatus for use in a computer system including a first memory and a second memory, the first memory including a plurality of bits tangibly embodied in the first memory at a plurality of positions, wherein b[i] refers to the bit at position i in the plurality of bits, the apparatus comprising:

means for selecting a first value for a current shift redundancy record variable tangibly embodied in the second memory, wherein the current shift redundancy record value may be toggled between the first value and a second value;

for each of a plurality of consecutive values of i:

means for toggling the value of the current shift redundancy record variable if bit b[i] is defective and bit b[i-1] is functional;

means for identifying a set of *n* consecutive defective bits tangibly embodied in the first memory and including bit b[i] if bit b[i] is defective and bit b[i-1] is functional; and

means for tangibly storing in a shift redundancy circuit a hint value in a hints record entry corresponding to bit b[i], the hint value indicating the number *n*; and

means for tangibly storing the current shift redundancy record value in the shift redundancy circuit in a shift redundancy record element corresponding to bit b[i].

Claim 21 (currently amended). The apparatus of claim 20, wherein the means for the current shift redundancy record value comprises means for tangibly storing a single-bit value in the shift redundancy record representing the position of bit b[i].

Claim 22 (original). The apparatus of claim 20, further comprising:

means for controlling switching circuitry to disconnect the set of *n* consecutive defective bits from input/output ports of the memory.